

Monolithic N-Channel JFET Duals

Product Summary

Part Number	$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	g_{fs} Min (mS)	I_G Max (pA)	$ V_{GS1} - V_{GS2} $ Max (mV)
U421	-0.4 to -2	-40	0.3	-0.25	10
U423	-0.4 to -2	-40	0.3	-0.25	25

Features

- Monolithic Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 0.2 pA
- Low Noise
- High CMRR: 102 dB

Benefits

- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

Applications

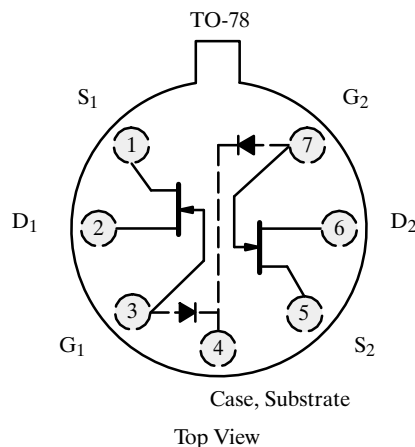
- Ultralow Input Current Differential Amps
- High-Speed Comparators
- Impedance Converters

Description

The U421/423 are monolithic dual n-channel JFETs designed to provide very high input impedance for differential amplification and impedance matching. Among its many unique features, this series offers operating gate current specified at -250 fA.

The hermetic TO-78 package is available with full military processing (see Military Information).

For similar products see the low-noise U/SST401 series and high-gain 2N5911/5912 data sheets.



Absolute Maximum Ratings

Gate-Drain, Gate-Source Voltage -40 V
 Gate-Gate Voltage ± 40 V
 Gate Current 10 mA
 Lead Temperature ($1/16$ " from case for 10 sec.) 300 °C
 Storage Temperature -65 to 200 °C
 Operating Junction Temperature -55 to 150 °C

Power Dissipation : Per Side^a 300 mW
 Total^b 500 mW

- Notes
- Derate 2.4 mW/°C above 25 °C
 - Derate 4 mW/°C above 25 °C

Specifications^a

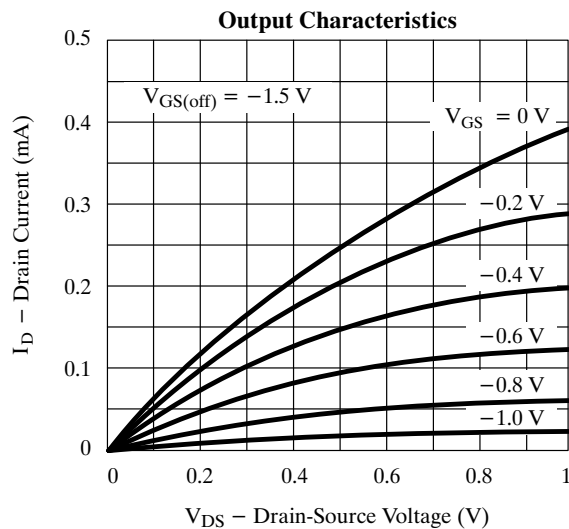
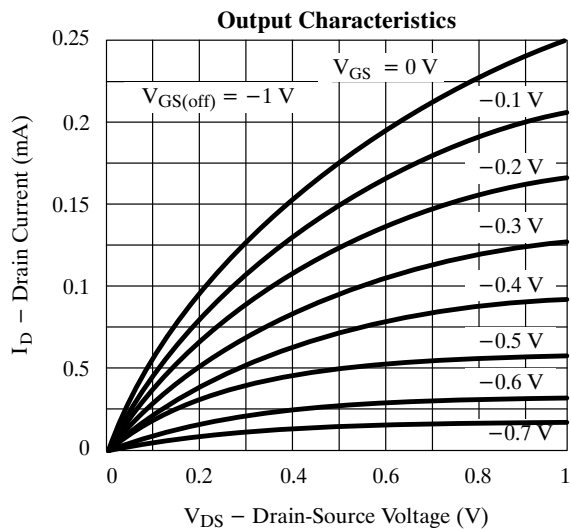
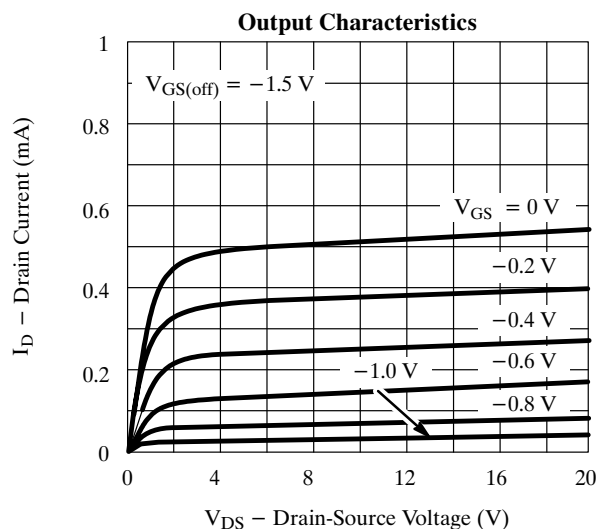
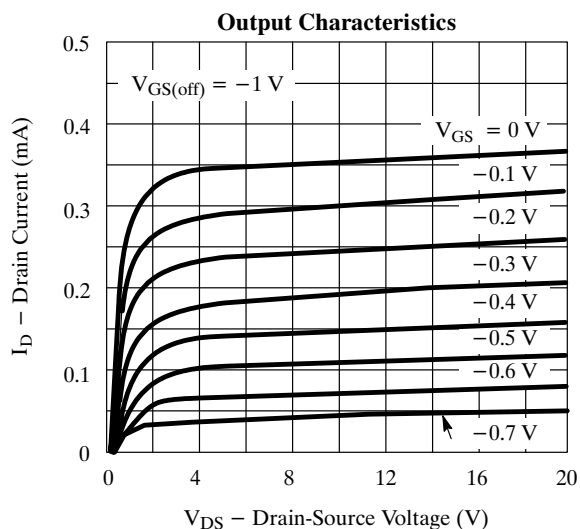
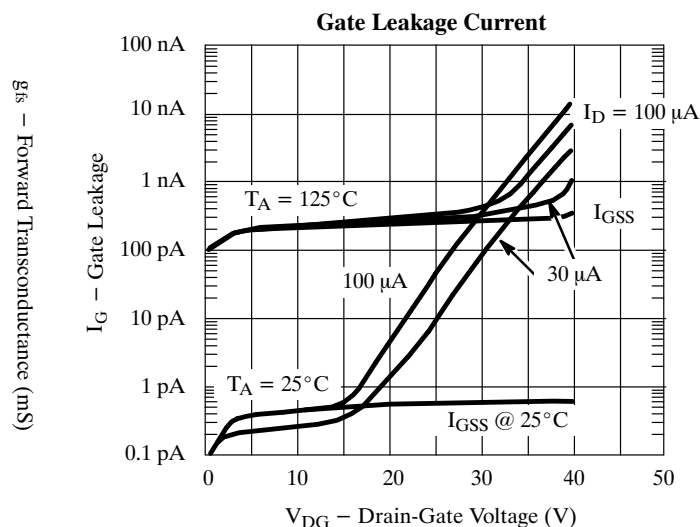
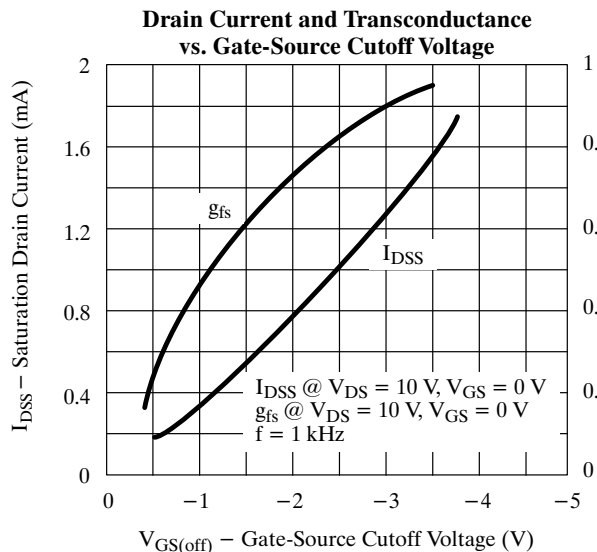
Parameter	Symbol	Test Conditions	Typ ^b	Limits				Unit
				U421		U423		
				Min	Max	Min	Max	
Static								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = -1 \mu A, V_{DS} = 0 V$	-60	-40		-40		V
Gate-Gate Breakdown Voltage	$V_{(BR)G1-G2}$	$I_G = \pm 1 \mu A, I_D = 0, I_S = 0$	± 55	± 40		± 40		
Gate-Source Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = 10 V, I_D = 1 nA$	-1.2	-0.4	-2	-0.4	-2	
Saturation Drain Current	I_{DSS}	$V_{DS} = 10 V, V_{GS} = 0 V$	400	60	1000	60	1000	μA
Gate Reverse Current	I_{GSS}	$V_{GS} = -20 V, V_{DS} = 0 V$ $T_A = 125^\circ C$	-0.6		-1		-1	pA
			-0.3		-1		-1	nA
Gate Operating Current	I_G	$V_{DG} = 10 V, I_D = 30 \mu A$ $T_A = 125^\circ C$	-0.2		-0.25		-0.25	pA
			-150		-250		-250	pA
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{GS} = 0 V, I_D = 10 \mu A$	2000					Ω
Gate-Source Voltage	V_{GS}	$V_{DG} = 10 V, I_D = 30 \mu A$	-0.8		-1.8		-1.8	V
Gate-Source Forward Voltage	$V_{GS(F)}$	$I_G = 1 mA, V_{DS} = 0 V$	0.7					
Dynamic								
Common-Source Forward Transconductance	g_{fs}	$V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz$	0.6	0.3	1.5	0.3	1.5	mS
Common-Source Output Conductance	g_{os}		4		10		10	μS
Common-Source Forward Transconductance	g_{fs}	$V_{DS} = 10 V, I_D = 30 \mu A, f = 1 kHz$	0.2	0.12	0.35	0.12	0.35	mS
Common-Source Output Conductance	g_{os}		0.4		3		3	μS
Common-Source Input Capacitance	C_{iss}	$V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz$	1.4		3		3	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.7		1.5		1.5	
Equivalent Input Noise Voltage	\bar{e}_n	$V_{DS} = 10 V, I_D = 30 \mu A$ $f = 10 Hz$	30		70		70	nV/\sqrt{Hz}
Noise Figure	NF	$R_G = 10 M\Omega$			1		1	dB
Matching								
Differential Gate-Source Voltage	$ V_{GS1} - V_{GS2} $	$V_{DG} = 10 V, I_D = 30 \mu A$			10		25	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	$V_{DG} = 10 V, I_D = 30 \mu A$ $T_A = -55 to 125^\circ C$			10		40	$\mu V/^\circ C$
Common Mode Rejection Ratio	CMRR	$V_{DG} = 10 to 20 V, I_D = 30 \mu A$	102	90		80		dB

Notes

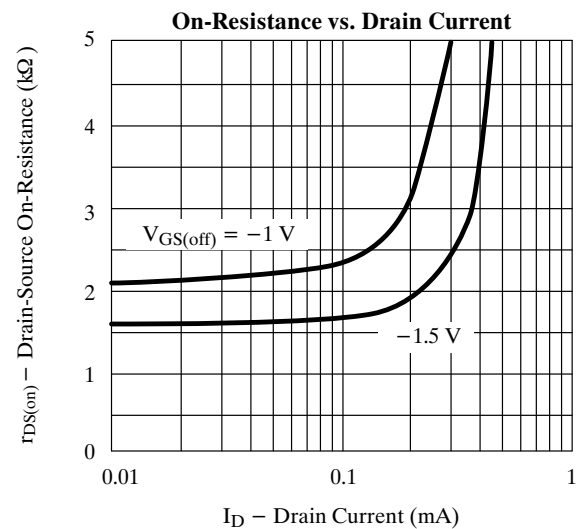
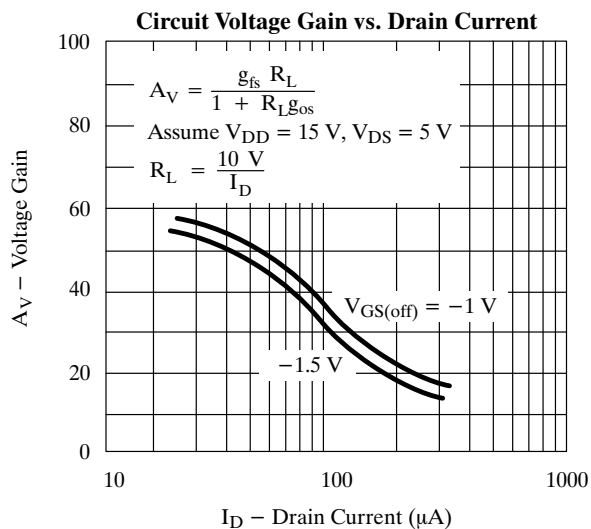
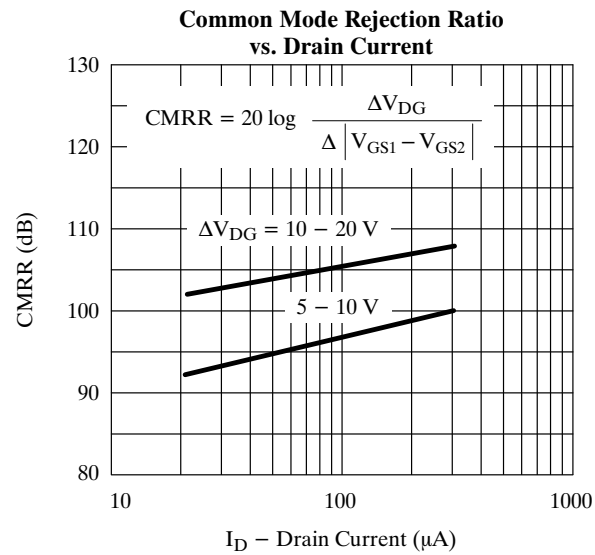
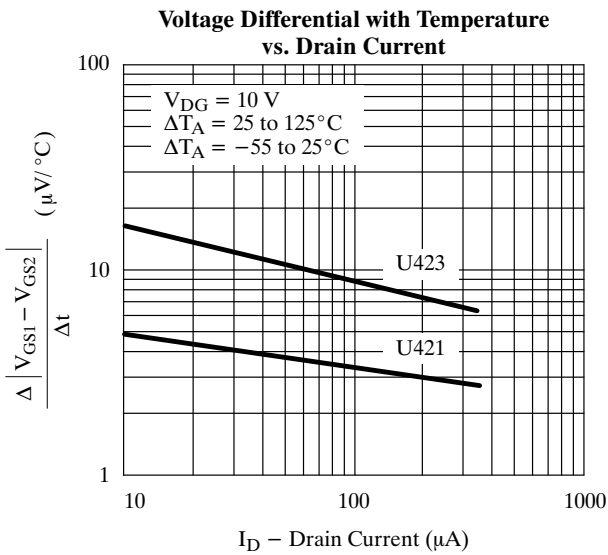
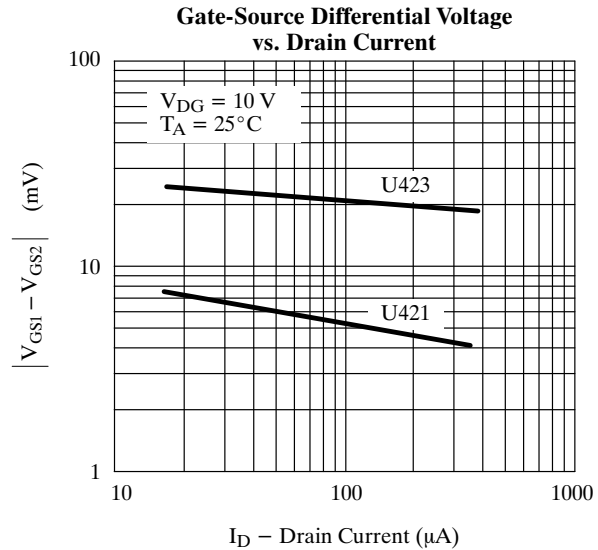
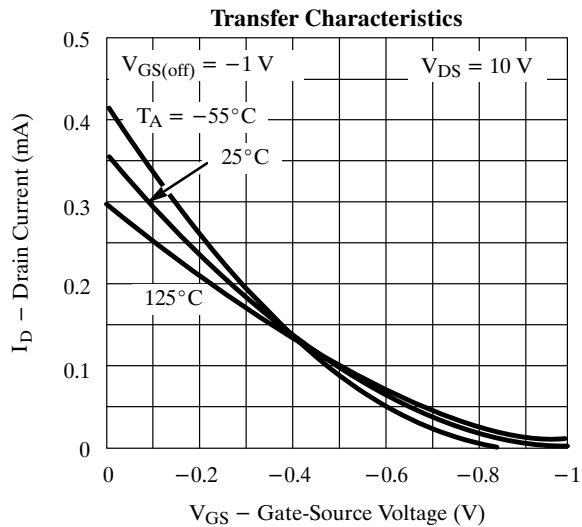
- a. $T_A = 25^\circ C$ unless otherwise noted.
 b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

NNT

Typical Characteristics



Typical Characteristics (Cont'd)



Typical Characteristics (Cont'd)

